

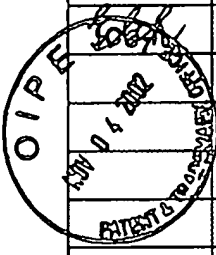
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Sheet 1 of 1

Substitute Form PTO-1449 (Modified) Information Disclosure Statement by Applicant (Use several sheets if necessary) (37 CFR §1.98(b))	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. 10559-614001	Application No. 10/020,815
	Applicant Gilbert Wolrich et al.		
	Filing Date December 12, 2001	Group Art Unit 2171	

U.S. Patent Documents

Examiner Initial	Desig. ID	Patent Number	Issue Date	Patentee	Class	Subclass	Filing Date If Appropriate
	AA	6,359,911 B1	3/19/2002	Movshovich et al.	—	—	
	AB						
	AC						
	AD						
	AE						
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Foreign Patent Documents or Published Foreign Patent Applications

Examiner Initial	Desig. ID	Document Number	Publication Date	Country or Patent Office	Class	Subclass	Translation	
							Yes	No
	AL							
	AM							
	AN							
	AO							
	AP							

Other Documents (include Author, Title, Date, and Place of Publication)

Examiner Initial	Desig. ID	Document
	AQ	
	AR	
	AS	
	AT	

Examiner Signature <i>E. P. Whouse</i>	Date Considered <i>7/19/04</i>
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Sheet 1 of 2

Substitute Form PTO-1449 (Modified) JUL 01 2004 PATENT & TRADEMARK OFFICE (37 CFR 1.98(b))	U.S. Department of Commerce Patent and Trademark Office		Attorney's Docket No. 10559-614001	Application No. 10/020,815
	Information Disclosure Statement by Applicant (Use several sheets if necessary)		Applicant Gilbert Wolrich, et al.	
			Filing Date December 12, 2001	Group Art Unit 2171 2161

U.S. Patent Documents							
Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
Eld	AA	09/475,614	12/30/1999	Wolrich et al.			
Eld	AB	09/473,571	12/28/1999	Wolrich et al.			

Foreign Patent Documents or Published Foreign Patent Applications								
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	AE	WO 01/48619	07/05/2001	WIPO				
	AF	WO 01/48606	07/05/2001	WIPO				
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Eld	AT	Byrd et al., "Multithread Processor Architectures," <i>IEEE Spectrum</i> , Vol. 32, No. 8, New York, 1 August 1995, pp. 38-46.
Eld	AU	Doyle et al., <i>Microsoft Press Computer Dictionary</i> , 2 nd ed., Microsoft Press, Redmond, Washington, USA, 1994, p. 326.

Examiner Signature <i>E. P. Lehane</i>	Date Considered 12/28/2005
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Substitute Form PTO-1449

U.S. Department of Commerce
Patent and Trademark Office

Attorney's Docket No.

Application No.

(Modified)

10559-614001

10/020815

**Information Disclosure Statement
by Applicant**

(Use several sheets if necessary)

Applicant

Gilbert Wolrich, et al.

Filing Date

December 12, 2001

Group Art Unit

2171

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	AW	Gomez et al., "Efficient Multithreaded User-Space Transport for Network Computing: Design and Test of the TRAP Protocol," <i>Journal of Parallel and Distributed Computing</i> , Academic Press, Duluth, Minnesota, USA, vol. 40, no. 1, 10 January 1997, pp. 103-117. ✓
	AX	Haug et al., "Reconfigurable hardware as shared resource for parallel threads," IEEE Symposium on FPGAs for Custom Computing Machines, 1998. ✓
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	AZ	Hyde, R., "Overview of Memory Management," <i>Byte</i> , vol. 13, no. 4, 1998, pp. 219-225. ✓
	AAA	Litch et al., "StrongARMing Portable Communications," IEEE Micro, 1998, pp. 48-55. ✓
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	AEE	Trimberger et al., "A time-multiplexed FPGA," Proceedings of the 5 th Annual IEEE Symposium on Field-Programmable Custom Computing Machines, 1998. ✓
	AFF	Turner et al., "Design of a High Performance Active Router," Internet Document, <i>Online</i> , 18 March 1999. ✓
	AGG	Vibhatavani et al., "Simultaneous Multithreading-Based Routers," Proceedings of the 2000 International Conference of Parallel Processing, Toronto, Ontario, Canada, 21-24 August 2000, pp. 362-359. ✓
✓	AHH	Wazlowski et al., "PRSIM-II computer and architecture," IEEE Proceedings, Workshop on FPGAs for Custom Computing Machines, 1993. ✓

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or 20030147409 or 20030140196 or
20030131198 or 20030131022 or 20030115347
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US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

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US Published Applications

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Signature

Examiner Name	Date
<i>E. J. W. Rouse</i>	<i>12/28/2005</i>